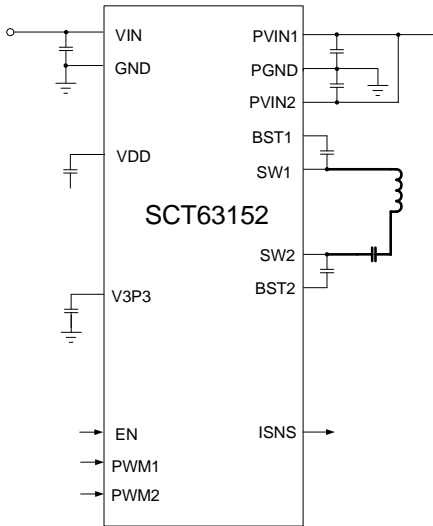


## 15W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

- VIN Input Voltage Range: 2.8V-20V
- PVIN Input Voltage Range: 1V-18V
- Up to 15W Power Transfer
- Integrated Full-Bridge Power Stage with 9m Rdson of Power MOSFETs
- Integrated 5V-100mA LDO
- Optimized for EMI Reduction
- Build-in 3.3V-100mA LDO
- Ultra-low quiescent current in Low IQ mode , IQ <15uA
- Integrated Lossless Input Current Sensor with  $\pm 2\%$  accuracy for FOD and current Demodulation
- Integrated voltage and current demodulation
- Integrated Q factor detection
- 3.3V and 5V PWM Signal Logic CoTJ ET Q EMC /Span <</MCID 143/Lang (en-US)>> BDC q 0.0000091221.57 438.0

# SCT63152



Low IQ mode quiescent current vs. Vin

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.  
 Revision 1.0: Released to Market.

| ORDERABLE DEVICE | PACKAGING TYPE | STANDARD PACK QTY | PACKAGE    |
|------------------|----------------|-------------------|------------|
|                  |                |                   | F6Q-EMC-SP |







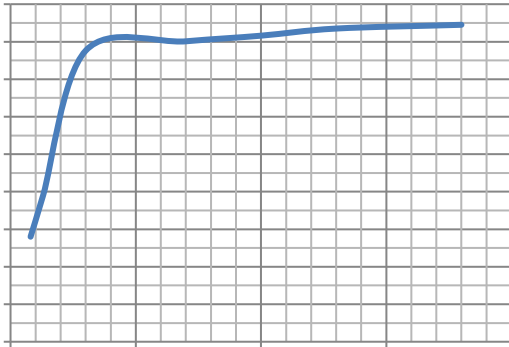


Figure 2. Low IQ mode current vs Vin

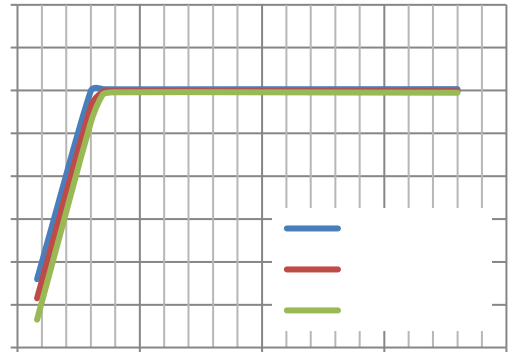


Figure 3. 5V LDO Vout vs Vin

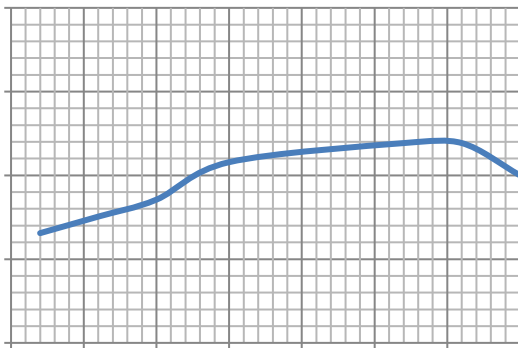


Figure 4. 5V LDO Vout vs temperature @ Vin=12V

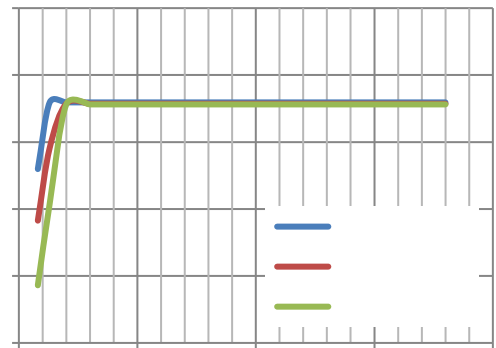


Figure 5. 3.3V LDO Vout vs Vin

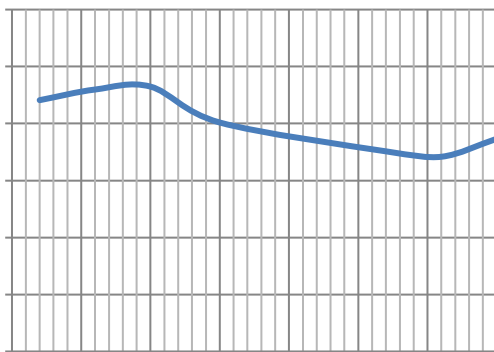


Figure 6. 3.3V LDO Vout vs temperature @ Vin=12V

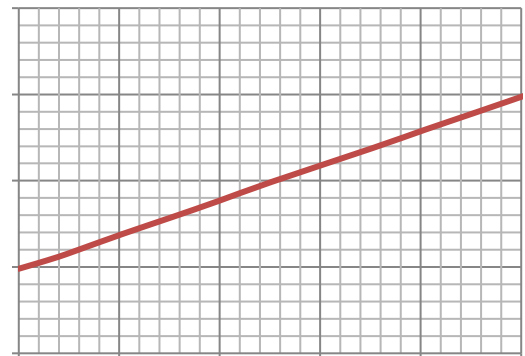


Figure 7. Current Sense Output Voltage vs Iin

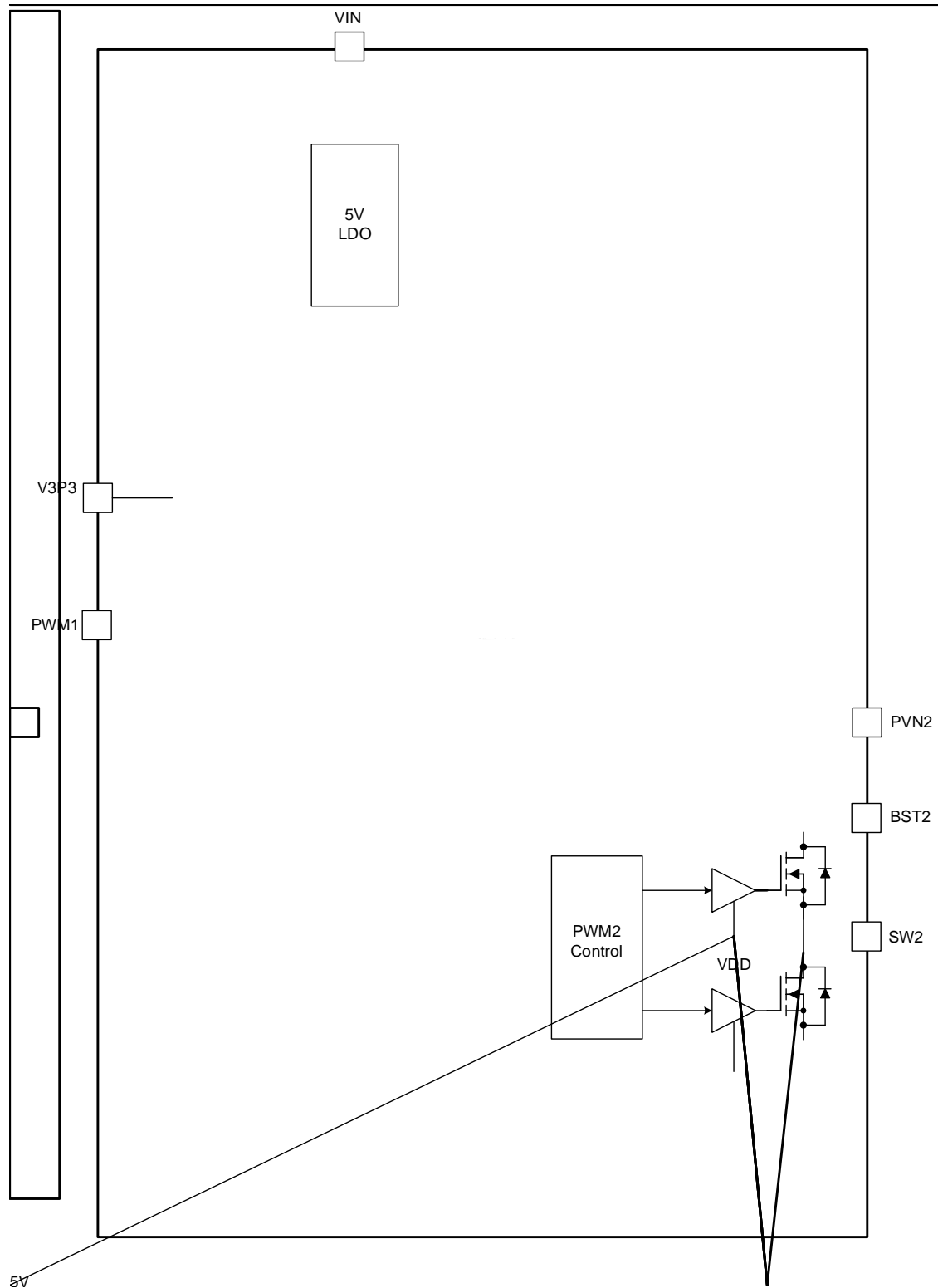


Figure 8. Functional Block Diagram

# SCT63152

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## Overview

The SCT63152 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1 gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot be kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

### Full Bridge Over Current Protection

The SCT63152 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 8A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in a high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 20ms typically.

### Current Sense

The SCT63152

## SCT63152

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It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

### Low IQ



Typical Application

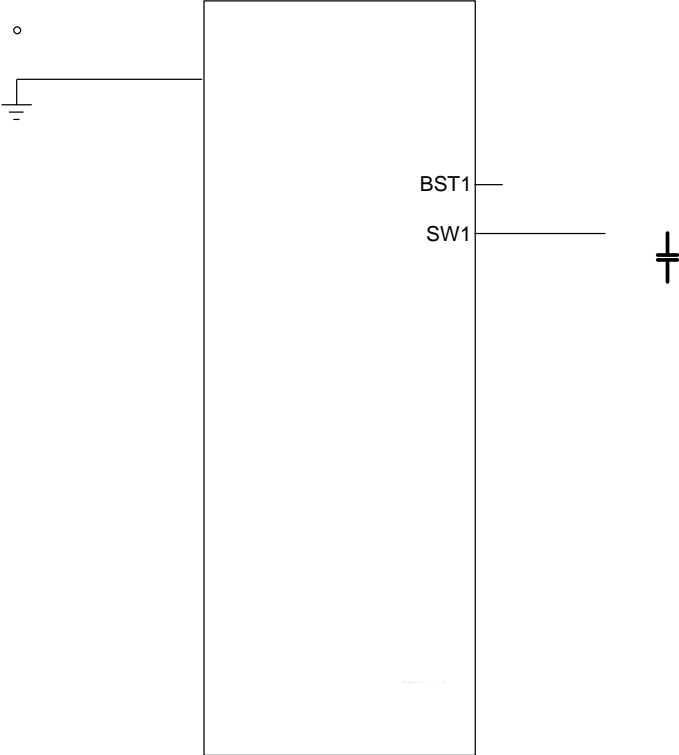


Figure 11. Same Input to VIN and PVIN



**Layout Guideline**



