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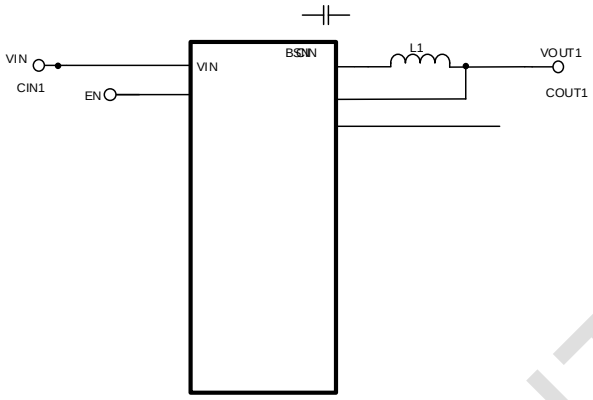
TYPICAL APPLICATION



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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to Market

Revision 1.1: Add slee mode and watchdog description, update thermal resistance and layout guideline, correct typo

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT61450S-xxxxFDAR(1)	Tape & Reel	5000	450S	24	FCTQFN4x4-24L	1
SCT61450S-0001FDAR	Tape & Reel	5000	450S	24	FCTQFN4x4-24L	1

1) “xxxx” is the specific suffix code for different configuration, contact SCT for details

PART NUMBER	CHIP_ID	CONFIG_T1	CONFIG_EN	CONFIG_PU1	CONFIG_PU2	VOUT2	VOUT3	I2C ADDRESS
SCT61450S-0001FDAR	41h	00h	3Dh	00h	11h	06h o 1 .1Vo	0Eh o 1 .5Vo	38h

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.5		36	V
$V_{IN_UVLO_RISING}$	Input UVLO rising threshold	VIN_START[1:0]=00b	3	3.2	3.4	V
		VIN_START[1:0]=01b	3.8	4	4.2	V
		VIN_START[1:0]=10b	4.8	5	5.2	V
		VIN_START[1:0]=11b	5.8	6	6.2	V
$V_{IN_UVLO_FALLING}$	Input UVLO falling threshold	VIN_STOP[1:0]=00b	2.5	2.8	3.1	V
		VIN_STOP[1:0]=01b	3.2	3.5	3.8	V
		VIN_STOP[1:0]=10b	4.2	4.5	4.8	V
		VIN_STOP[1:0]=11b	5.2	5.5	5.8	V
V_{IN_OVP}	Input OVP	V_{IN} rising	40	43	45	V
$V_{IN_OVP_HYS}$	Hysteresis			3		

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

I2C Interface				
V_{IH}	High-level input voltage		1.2	V
V_{IL}	Low-level input voltage		0.4	V
V_{OL}	Low-level output voltage	I_{SINK}=4mA	0.4	V
F_{SCL}(1)	SCL clock frequency		1	MHz
T_{LOW}(1)	Low period of the SCL clock		500	ns
T_{HIGH}(1)	High period of the SCL clock		260	ns
T_{HD_STA}(1)	Hold time (repeated) START condition		260	ns
T_{SU_STA}(1)	Set-up time (repeated) START condition		260	ns
T_{HD_DAT}(1)	Data hold time		0	ns
T_{SU_DAT}(1)	Data set-up time		50	ns

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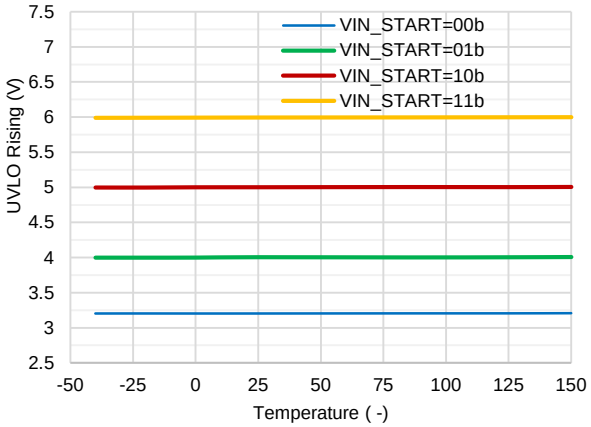
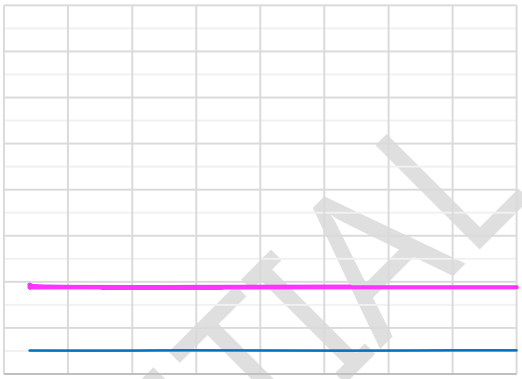
TYPICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



UVLO Rising Threshold vs. Temperature



UVLO Falling Threshold vs. Temperature

VCC vs. Temperature

Buck1 R_{DSON_HS1} vs. Temperature

Buck1 R_{DSON_LS1} vs. Temperature

Buck2 R_{DSON_HS2} vs. Temperature

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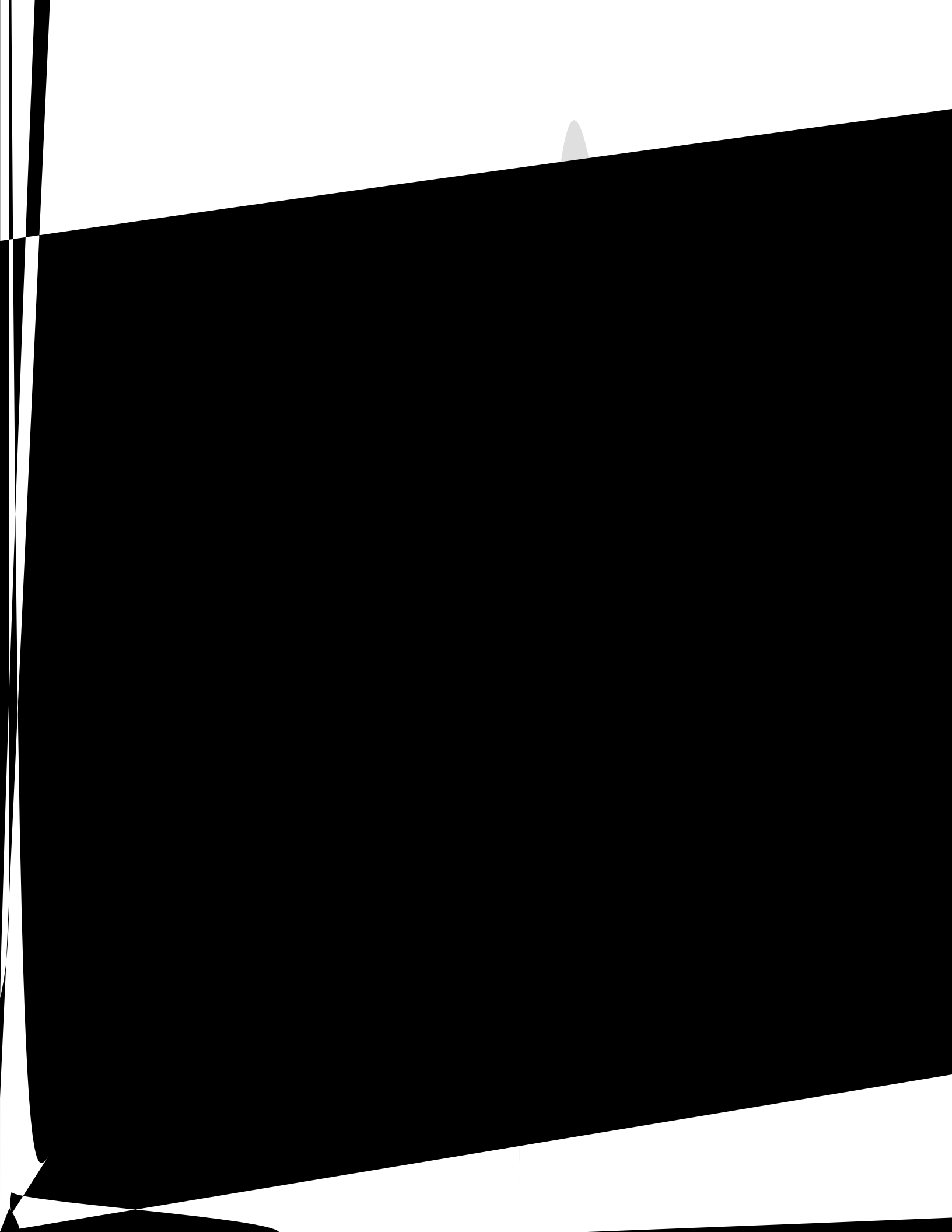

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rail on, other rails are optional depending on register **CONFIG_ENLP**. Most unnecessary circuits will turn off to save power consumption. Deep safe event is still valid to provide protection. Note the RESETB pin is still high during this state to keep MCU alive. Once SLEEPB pin is pulled high longer than deglitch time, the device will exit from sleep mode and go to RECOVER state. The rest channels will then recover.

RECOVER State

Once the device is awake from sleep mode, the RECOVER state is an intermediate state before device go back to NORMAL state. The channels which are disabled in SLEEP state will start up according to programmed turn on delay. After all output are built up successfully, the device will then enter NORMAL state. If there is reset event during RECOVER state, the device will go to RCVRST state.

RCVRST State

RCVRST state is extra reset state to assert RESETB pin, other rails will still start up in programmed sequence. This state aims to provide possible reset events including OV/UV and watchdog detection for those continuously enabled rails. The device will go back to RECOVER state automatically after once the holding time is expired and no reset event.

VIN and EN UVLO

When the VIN pin voltage rises above 3.2V and the EN pin voltage exceeds the enable threshold of 1.2V, the device is enabled. And the device disables when the VIN pin voltage falls below 2.8V or when the EN pin voltage is below 1.0V.

EN pin is connected internally to ground allows the device to be disabled when EN pin is floating to simplify the system design.

High Efficiency Regulators

The switching frequency of HV Buck is 2.2MHz/400kHz selectable. Allv.1 (612 (v)4 (o-0.00cs 1 0 0 scn 0-0.c -0.01 T(LVto)Tj 0

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I2C Interface

The SCT61450S integrates a two-wire serial interface for bidirectional communications between the device and the master through bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The SCT61450S is always assigned a unique chip address and operates as a slaver, the master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and SDA lines need a pull-up resistor connected to bus voltage since HIGH state is the default state when bus is idle. The SCT61450S

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Application Waveforms (continued)

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.15V, V_{OUT3}=1.5V, V_{OUT4}=5V, V_{OUT5}=3.3V,unless otherwise noted

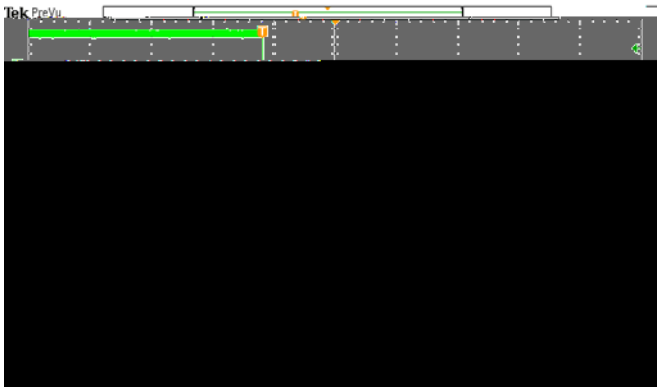

Figure 17. EN Off (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

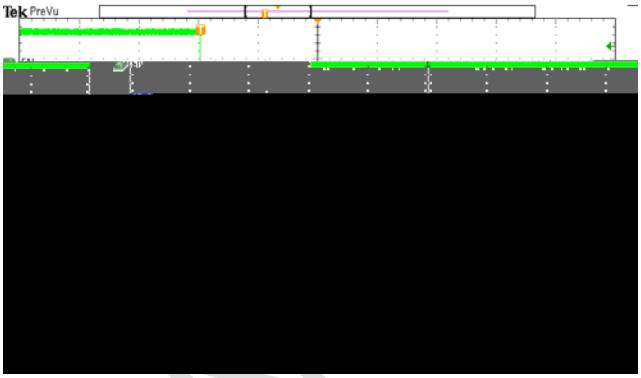

Figure 18. EN Off (Io2=Io3=2A, Io4=0.5A, Io5=0.8A)

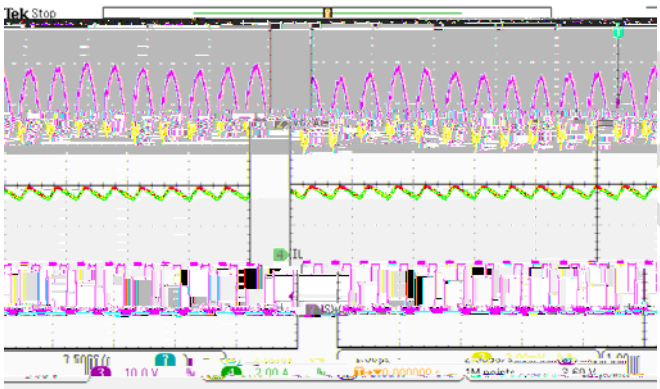

Figure19. Buck1 Steady State (Io1 = 3A)

Figure 20. Buck2 Steady State (Io2 = 2A)

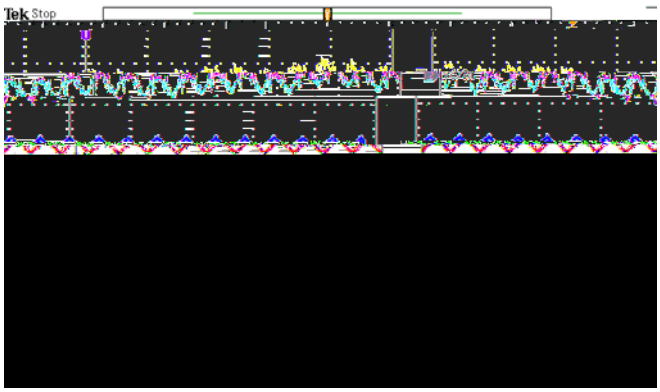

Figure 21. Buck3 Steady State (Io3 = 2A)

Figure 22. Boost4 Steady State (Io4 = 500mA)

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Register Map

ADDRESS	REGISTER	DEFAULT VALUE	OTP ACCESS	I2C LOCK	WD LOCK
0x00	CHIPID	-	Y	N	N
0x01	CONFIG_FSS	70h	Y	Y 999.3 696 (T)-8.604 T.3 681 0.9 0.959 9 e f 21	

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STATUV [7:0]				
ADDRESS: 0x0A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	UV	Read Clear	UV Comparator Status for all channels with Digital Filter.	0 = All enabled channels are above UV threshold after DF 1 = Any enabled channel is below UV threshold after DF
[6]	RESERVED	R	/	/
[5]	UV_WAR5	Read Clear	UV warning for OUT5, Digital Filter is not included	0 = OUT5 is above UV threshold before DF 1 = OUT5 is below UV threshold before DF

UV_WAR5 Read

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[2]	OV_WAR2	Read Clear	OV warning for OUT2, Digital Filter is not included	0 = OUT2 is below OV threshold before DF 1 = OUT2 is above OV threshold before DF
[1]	OV_WAR1	Read Clear	OV warning for OUT1, Digital Filter is not included	0 = OUT1 is below OV threshold before DF 1 = OUT1 is above OV threshold before DF
[0]	RESERVED	R	/	/

STATOFF [7:0]				
ADDRESS: 0x0C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	OFF5	Read Clear	OFF Comparator Status for OUT5	0 = OUT5 is above OFF threshold 1 = OUT5 is below OFF threshold
[4]	OFF4	Read Clear	OFF Comparator Status for OUT4	0 = OUT4 is above OFF threshold 1 = OUT4 is below OFF threshold
[3]	OFF3	Read Clear	OFF Comparator Status for OUT3	0 = OUT3 is above OFF threshold 1 = OUT3 is below OFF threshold
[2]	OFF2	Read Clear	OFF Comparator Status for OUT2	0 = OUT2 is above OFF threshold 1 = OUT2 is below OFF threshold
[1]	OFF1	Read Clear	OFF Comparator Status for OUT1	0 = OUT1 is above OFF threshold 1 = OUT1 is below OFF threshold
[0]	RESERVED	R	/	/

STATD [7:0]				
ADDRESS: 0x0D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RESERVED	R	/	/
[6]	CLK_ERR	Read Clear	CLK fault indicator	0 = No fault detected 1 = CLK error detected
[5]	SUP_ERR	Read Clear	Supply fault indicator, include VCC OV fault and VIN OV fault	0 = No fault detected 1 = VCC OV or VIN OV detected
[4]	RST_ENTER	Read Clear	RESET state indicator	0 = No fault detected 1 = RESET state has entered since the last read.
[3]	DEEPSAFE_ENTER	Read Clear	DEEPSAFE state indicator	0 = No fault detected 1 = DEEPSAFE state has entered since the last read.
[2]	PIN_ERR	Read Clear	Pin fault indicator, include RESETB Pin stuck fault and GND pin LOSS fault	0 = No fault detected 1 = RESETB Short to supply detected or pull-down fail or GND LOSS since the last read
[1]	THSD	Read Clear	Thermal Shutdown Indication	0 = No thermal shutdown 1 = Thermal shutdown has occurred since last read
[0]	INTERR	Read Clear	Internal Error, include OTP CRC failure and ABIST failure	0 = No internal error detected 1 = Internal error detected

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STATWD [7:0]				
ADDRESS: 0x0E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	RESETB_STAT	R	RESETB Pin State. Allows verification of the state of the RESETB pin. This is the real-time RESETB pin state.	0 = RESETB is low 1 = RESETB is high
[4]	WD_OPEN	R	Watchdog Open Window. This bit indicates that it is permissible to update the watchdog. This bit shows real-time status.	0 = Watchdog update not open 1 = Watchdog ok to update
[3]	WD_ERR	R	Watchdog ERROR for 1 time or 2 times (config by WD_FAIL_CNT), LFSR mismatch is not included	0 = No error detected 1 = Error detected
[2]	WD_LFSR	Read Clear	LFSR Write Mismatch. The MCU/SoC did not write the correct value to the WDKEY register.	0 = LFSR key match 1 = LFSR key mismatch since last read
[1]	WD_UV	Read Clear	Watchdog Update Violation. The MCU/SoC wrote to the WDKEY register during the CLOSE window.	0 = No violation detected 1 = Watchdog updated too early
[0]	WD_EXP	Read Clear	Watchdog Open Window Expired. The MCU/SoC did not write to the WDKEY register during the whole window.	0 = Watchdog timer not expired 1 = Watchdog timer expired

VOUT2 [7:0]				
ADDRESS: 0x0F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4:0]	OUT2	W/R	OUT2 Voltage Setting	VOUT2 = OUT2[4:0] x 50mV + 0.8V (0.8V to 2.35V)

VOUT3 [7:0]				
ADDRESS: 0x10				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4:0]	OUT3	W/R	OUT3 Voltage Setting	VOUT3 = OUT3[4:0] x 50mV + 0.8V (0.8V to 2.35V)

CONFIG_MISC [7:0]				
ADDRESS: 0x11				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4]	VIN_OVP_EN	W/R	Enable of VIN OVP. When VIN>43V, part enter DEEPSAFE mode.	0 = Disabled 1 = Enabled
[3:2]	VIN_START	W/R	VIN start threshold at VIN rising	00 = 3.2V; 01 = 4V; 10 = 5V; 11 = 6V
[1:0]	VIN_STOP	W/R	VIN stop threshold at VIN falling	00 = 2.8V; 01 = 3.5V; 10 = 4.5V; 11 = 5.5V

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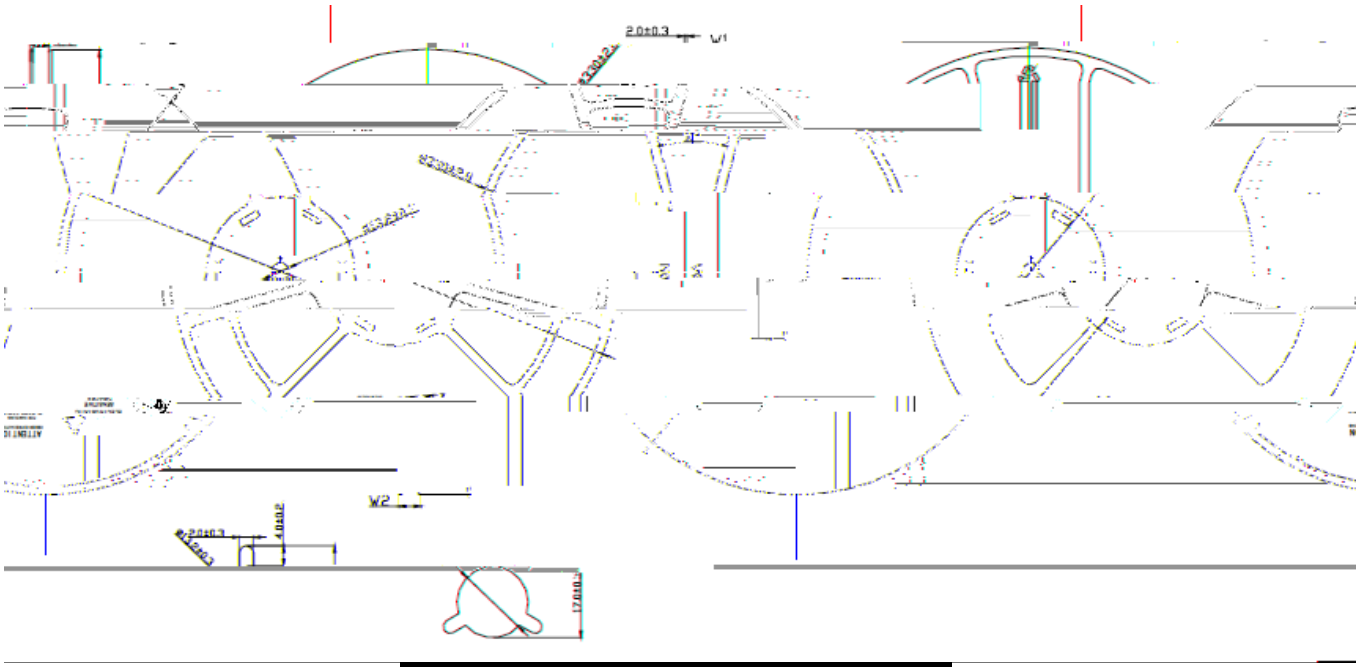
TAPE AND REEL INFORMATION



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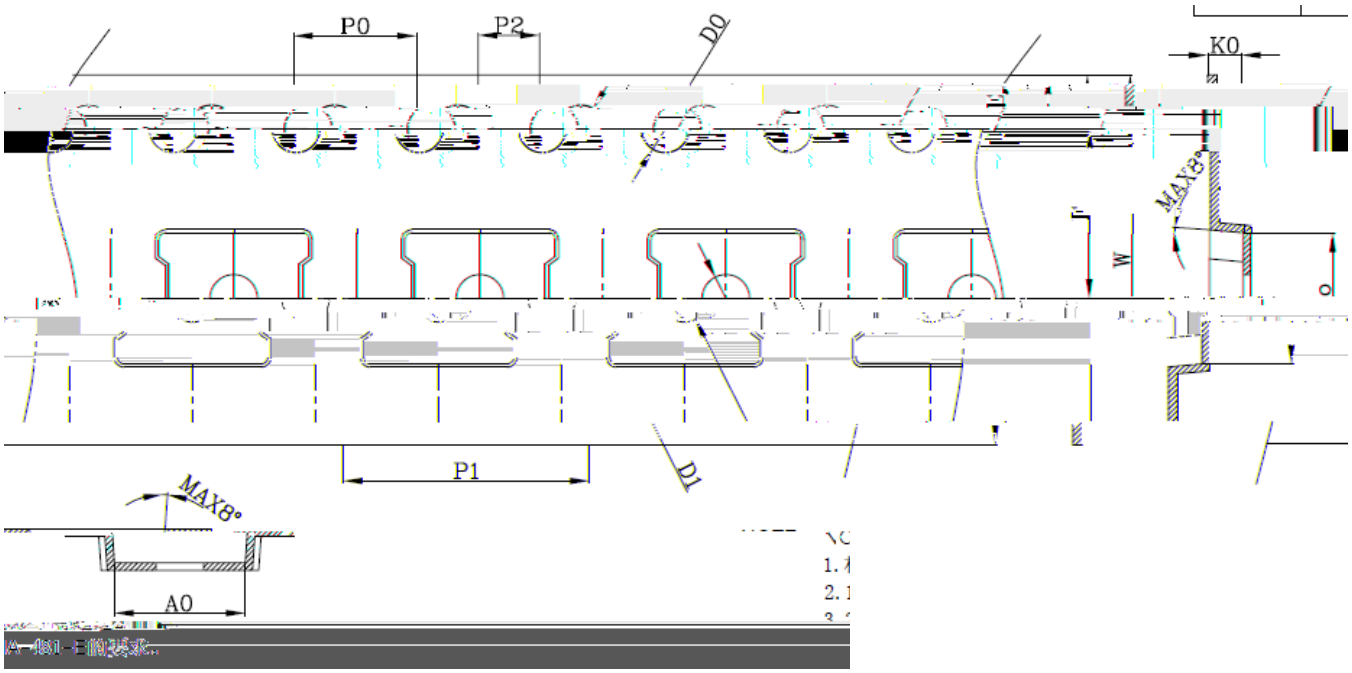

SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	1.10±0.10	4.00±0.10	8.00±0.10	2.00±0.05	4.00±0.10	2.00±0.10	4.30±0.10	4.30±0.10

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